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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,282	02/20/2004	Shin-ichiro Fukai	10873.1405US01	7603

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EXAMINER	
CODY, DILLON J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,282	FUKAI ET AL.	
	Examiner	Art Unit	
	Dillon J. Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) *10* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/3/2004, 1/3/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, drawings, and declaration, all filed 20 February 2004; and information disclosure statements filed 3 May 2004 and 3 January 2006.

Priority

3. Applicant's claim for foreign priority date of 24 February 2003 is hereby acknowledged.

Election/Restrictions

4. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-9, drawn to a processor performing a function, classified in class 712, subclass 229.

II. Claim 10, drawn to a compiler implementing code for the processor of group I, classified in class 717, subclass 140

The inventions are distinct, each from the other because of the following reasons:

5. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not

overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination II has separate utility such as generating code for use on a processor different than that claimed in Group I. See MPEP § 806.05(d).

6. Because these inventions are independent or distinct for the reasons given above and have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

7. Because these inventions are independent or distinct for the reasons given above and the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

8. During a telephone conversation with Douglas Mueller (#30,300) on 13 April 2006 a provisional election was made with traverse to prosecute the invention of group I, claims 1-9. Affirmation of this election must be made by applicant in replying to this Office action. Claim 10 is withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Title

9. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Specification

10. The abstract of the disclosure is objected to because

Line 8: "a" should follow "When"

11. Correction is required. See MPEP § 608.01(b).

12. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

13. Claims are objected to because of the following informalities:

Claim 6, line 1: "claims 3" should read "claim 3".

Claim 6, line 2: "the instruction code" should read "an instruction code" as "instruction code" has not been disclosed in a prior claim.

14. Appropriate correction is required.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Mahon et al. (U.S. Patent No. 4,809,160) hereinafter referred to as Mahon.

17. As per claim 1, Mahon teaches a processor comprising:

a CPU;

an instruction memory for storing a program; (Fig. 4 memory 410)

and an invalid branch detection unit, wherein when a branch instruction that changes an operation mode to another operation mode is executed by the program stored in the instruction memory, the invalid branch detection unit determines whether there is a branch enable instruction (Fig. 4 gateway instruction 430) in a branch destination address, and in the presence of the branch enable instruction, the invalid branch detection unit permits a change in operation mode, while in the absence of the branch enable instruction, the invalid branch detection unit outputs an invalid branch detection signal. (Col. 3 lines 16-68)

18. As per claim 2, Mahon teaches the processor according to claim 1, further comprising:

an execution area judgment unit that judges an execution area from a value of a program counter of an instruction executed by the CPU;

an executive operation mode decision unit that decides an executive operation mode in accordance with the judgment of the execution area judgment unit; *The examiner asserts that Mahon's processor inherently contains logic to*

detect the privilege level of the current code segment and of that of a target code segment and logic to detect a change in privilege level, as described in col. 1 line 55 – col. 2 line 45.

a branch destination area judgment unit that judges a branch destination area from a value of a branch destination address when a branch instruction is executed by the program stored in the instruction memory;

a branch destination operation mode decision unit that decides a branch destination operation mode in accordance with the judgment of the branch destination area judgment unit; *The examiner asserts that Mahon's processor inherently contains logic to detect what region of code is currently running and to what region a branch is directed. Further, the logic must detect what privilege level the region requires to run, as described in col. 1 line 55 – col. 2 line 45.*

and an operation mode change detection unit that detects a change in operation mode by comparing the executive operation mode decided by the executive operation mode decision unit with the branch destination operation mode decided by the branch destination operation mode decision unit, (Col. 1 line 55 – col. 2 line 45)

wherein when a branch instruction is executed by the program stored in the instruction memory while there is not a branch enable instruction in the branch destination address, the invalid branch detection unit outputs the invalid branch detection signal on condition that the operation mode change detection unit detects a change in operation mode. (Col. 2 line 19-24) *The examiner*

asserts that the "software trap" must be triggered by a logic line in the processor (invalid branch detection signal).

19. As per claim 3, Mahon teaches the processor according to claim 2, wherein when a branch instruction is executed by the program stored in the instruction memory while there is not a branch enable instruction in the branch destination address, the invalid branch detection unit outputs the invalid branch detection signal on condition that the operation mode change detection unit detects a change in operation mode, and the change in operation mode detected by the operation mode detection unit does not coincide with any change in operation mode specified by the branch enable instruction. (Col. 1 line 55 – col. 2 line 45)

20. As per claim 4, Mahon teaches the processor according to claim 1, wherein a specific instruction code that does not coincide with any other instructions is assigned to the branch enable instruction. *The examiner asserts that Mahon's processor must inherently use differing opcodes to designate a gateway instruction from any other instruction. If there were not different designations, the processor could not function correctly.*

21. As per claim 5, Mahon teaches the processor according to claim 1, wherein an instruction code that corresponds to at least one of other instructions is assigned to the branch enable instruction. *Mahon teaches having a gateway*

instruction for each page of memory (col. 4 lines 7-17). Each of these multiple instances of the gateway instruction will inherently share opcodes, as each is a gateway instruction.

22. As per claim 6, Mahon teaches the processor according to claim 3, further comprising a branch enable instruction code conversion unit that converts [an] instruction code of a branch enable instruction into an instruction code that corresponds to other instructions by detecting the branch enable instruction. (Col. 3 lines 61-68)

23. As per claim 7, Mahon teaches the processor according to claim 1, further comprising an interrupt output unit that outputs an interrupt request to the CPU by detecting the invalid branch detection signal output from the invalid branch detection unit. (Col. 3 lines 46-50)

24. As per claim 8, Mahon teaches the processor according to claim 1, further comprising a reset output unit that outputs a reset signal to the CPU by detecting the invalid branch detection signal output from the invalid branch detection unit. (Col. 3 lines 46-50

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mahon.

27. As per claim 9, Mahon teaches the processor according to claim 1, but fails to disclose it further comprising an instruction conversion unit that converts an instruction in a branch destination address into an undefined instruction by detecting the invalid branch detection signal output from the invalid branch detection unit.

28. Official Notice is taken that converting an instruction to a no-op instruction is well known in the art. Changing a pending instruction to a no-op is a simple method of ignoring the instruction which takes little overhead and can be accomplished in a single clock-cycle.

29. It would have been obvious to one of ordinary skill in the art at the time of invention to have converted a pending branch into a no-op when it was to be ignored, as described in col. 3 lines 46-50, for the benefit of being a simple, low-cost method of ignoring the branch without causing undesired operation of the processor.

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kahle et al. (U.S. Patent No. 5,764,969) disclose a system using an "enable special access" instruction to allow instructions to execute when changing priority levels in execution.

31. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

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